

# Overview of VHDL Courses

For detailed course outlines and instructor write-ups visit our website: [www.tm-associates.com](http://www.tm-associates.com)

- **VHDL Introduction - 2 days**

**Basic Level, 70% Lecture, 30% Labs**

This two-day fast-track primer course in VHDL is recommended for the broader corporate audience including application engineers, R&D personnel, hotline engineers, technical writers, and engineering managers. People whose role demands the ability to read VHDL code, understand VHDL-specific issues, identify inefficient or non-synthesizable constructs, and support those who write code will benefit from this course. Both synthesis and simulation aspects of the language are covered. Practical lab exercises provide course participants with direct insight into how the capabilities of the language are used to develop and verify complex ICs, using today's EDA tools.

- **VHDL For Hardware Designers - 4 days**

**Basic Level, 50% Lecture, 50% Labs**

VHDL is a feature-rich hardware description language, well suited to the synthesis and verification of complex system-on-a-chip ASICs and FPGAs. This course is a hardware-oriented VHDL primer for the digital design or verification engineer. Through real-world lecture insights and lab examples, participants in this comprehensive, hands-on course will learn to write synthesis-friendly, simulator-efficient code for progressively more complex logic blocks. They'll acquire confidence in utilizing the more powerful aspects of the language, while gaining mastery over its intricacies. The course focuses 70% on RTL code for synthesis, and 30% on testbench code for simulation.

- **Advanced VHDL Coding Styles - 3 days**

**For Synthesis & Verification**

**Advanced Level, 50% Lecture, 50% Labs**

Synthesis and verification are key to successful ASIC and FPGA design. This course addresses a wide range of VHDL design areas integral to the design process. The course explores, in a tool independent format, methodology issues and examples, VHDL coding and modeling guidelines for synthesizable design and design verification. Lecture sessions are supported by multiple VHDL examples for each topic and are reinforced by application specific labs. Additional topics include creating synthesizable code for control, datapath, and FSM oriented designs. Creating verification environments and testbenches of varying complexity are fully explained. Additional topics include VHDL commenting guidelines, effective use of VHDL data types, and design for reuse issues.

### **About TM Associates**

Since 1996 TM Associates has specialized in providing the highest quality Verilog and VHDL training courses. All of our instructors are experienced hardware designers. Each course is developed by a team of Verilog or VHDL experts with many years of experience in hardware design, teaching and course development. Since its inception, TM Associates has delivered over 450 courses for technology companies throughout the world.