

## **VHDL Course Developers and Instructors**

TM Associates (TMA) believes that the best training is developed and delivered by people who are not only language experts but also have years of design experience. And instead of relying on one person and a single point of view TMA uses the team approach to develop training.

TMA has assembled a group of VHDL experts with over 50 years of VHDL experience. The following people developed our VHDL training.

### **Peter Ashenden**

Dr. Peter Ashenden is a recognized expert in the VHDL language. He has been actively involved in IEEE working groups developing VHDL standards. At the present time he serves in the following capacities:

- Standards Editor and Member of Editorial Board for “IEEE Design & Test of Computers”
- Vice Chair of IEEE Design Automation Standards Committee
- Co-editor of Series in Systems on Silicon for Morgan Kaufmann Publishers
- Member of System-Level Design Language Committee of Accellera and European CAD Standards Initiative
- Member of IEEE Design Automation Standards Committee and four working groups

In addition, Dr. Ashenden is also involved in the development of the Rosetta system-level design language, and is Technical Editor for the Draft Standard Rosetta Language Reference Manual being prepared by the Accellera SLDS Rosetta Committee.

Dr. Ashenden is a prolific author on VHDL. His work includes the following:

Books ( Morgan Kaufman, Publisher):

- *System Designer’s Guide to VHDL-AMS*
- *Designer’s Guide to VHDL, second edition*
- *Student’s Guide to VHDL*

Reports – 22

Publications – 33

Workshops – 5

Research Grants - 7

Dr. Ashenden received his B.Sc.(Hons) and Ph.D. from Adelaide University, South Australia. He is an independent consultant specializing in electronic design automation (EDA). His research interests are electronic design automation and computer architecture. He is a Senior Member of the IEEE and a member of the ACM.

### **Patrick McCabe**

Patrick (Pat) McCabe has over 20 years of ASIC, FPGA and system design experience. Mr. McCabe has extensive experience with top-down design techniques, verification, system simulation, behavioral model development, hardware/software co-simulation and co-verification, coverage measurement tools, and performance measurement techniques. In addition, he is highly experienced with Synopsys tools and the ModelSim simulator, and has been using VHDL and Synopsys since 1989. In addition to gate-array and full-custom design experience using IBM, NEC, and proprietary technologies, his FPGA experience includes the use of Xilinx, Altera, and Actel FPGA's. In addition, he has used 3rd party IP cores from various companies, including embedded ARM microprocessor cores.

Mr. McCabe has worked for various companies, including Intel, IBM, Cirrus Logic, Honeywell, and was also a founder of Basis Communications. His experience ranges from communications systems, to state-of-the-art microprocessor design, to space-borne computers, to industrial controls. Mr. McCabe has been responsible for the creation of a VHDL-based design methodology at a number of companies. On various projects, Mr. McCabe has held positions of lead hardware engineer, lead verification engineer and lead systems engineer. Mr. McCabe has also taught internal classes at various companies on VHDL-based design techniques.

Mr. McCabe has presented papers on bus functional model design and system simulation at the VHDL International User's Forum (VIUF), and has also been a session chair for that conference.

Mr. McCabe holds both Bachelor of Science and Master of Science degrees in Computer Engineering. He holds a U.S. patent for the design of a frame relay ASIC, and is also a member of the IEEE.

### **Ken Banas**

Ken Banas has been involved in ASIC and FPGA work for over 14 years. He has been involved in all aspects of the design process including process setup and documentation, design definition and documentation, RTL design and verification, synthesis, and static timing. His most recent emphasis is on timing closure for high-speed multi-million gate chips. His design experience has been with both VHDL and Verilog and he has taught numerous internal design process classes throughout his career. Mr. Banas has extensive experience with RTL, behavioral, and structural HDL design techniques using both synchronous and asynchronous methods. His specialty has been to understand the complete

design process. He has lead all steps of the process from product conception to chip and system validation in the lab.

Mr. Banas is currently focusing on state of the art timing closure techniques for complex chips involving dozens of clock domains, numerous hard and soft IP macros, with data rates in the multiple-gigahertz range. He has thorough knowledge of high speed synthesis techniques including physical synthesis.

Mr. Banas has worked for IBM, GE, Honeywell, Paradyne Corp., Cirrus Logic, Basis Communications and Intel. His responsibilities have ranged from ASIC designer to Lead Electrical Engineer for a military missile computer which included multiple boards and ASICs.

Mr. Banas has an M.S.E.E. from the University of South Florida and a B.S.E.E from Syracuse University. He holds a U.S. patent for the design of a DSL modem packet-processing ASIC, and is also a member of the IEEE.