

Verilog Verification Course Developers and Instructors

TM Associates (TMA) believes that the best training is developed and delivered by people who are not only subject matter experts but also have years of design experience. And instead of relying on one person and a single point of view TMA uses the team approach to develop training.

TMA has assembled a group of verification experts with over 49 years of experience. The following people developed our Verilog Verification training.

Chris Macionski, Bright Eyes Consulting

Chris Macionski has been designing and verifying ICs since 1994. Over the years, he has worked on a broad spectrum of designs, including telecom, datacom, processor, and video coprocessors. This experience has given Mr. Macionski the insight to see what techniques work across all designs and which are suited for a particular application.

Mr. Macionski is the President of Bright Eyes Consulting (<http://www.brighteyesconsulting.com>). He has taught Verilog, VHDL, and Specman Elite classes across North America and Europe.

Prior to joining Bright Eyes Consulting, Mr. Macionski was a Principal Engineer at Qualis Design and a Senior Consulting Engineer at Cadence Design Systems.

Mr. Macionski has presented papers at verification conferences. His papers include

- Shotgun E - An Eight Step Approach to Experience Random Verification
- Driving Reset on the Specman Highway: Rules of the Road

Mr. Macionski's primary focus over the years has been verification of SOC and creating verification IP.

Patrick McCabe, Seaside Consulting

Patrick (Pat) McCabe has over 20 years of ASIC, FPGA and system design experience. Mr. McCabe has extensive experience with top-down design techniques, verification, system simulation, behavioral model development, hardware/software co-simulation and co-verification, coverage measurement tools, and performance measurement techniques. In addition, he is highly experienced with Synopsys tools and the ModelSim simulator, and has been using VHDL and Synopsys since 1989. In addition to gate-array and full-custom design experience using IBM, NEC, and proprietary technologies, his FPGA experience includes the

use of Xilinx, Altera, and Actel FPGA's. In addition, he has used 3rd party IP cores from various companies, including embedded ARM microprocessor cores.

Mr. McCabe has worked for various companies, including Intel, IBM, Cirrus Logic, Honeywell, and was also a founder of Basis Communications. His experience ranges from communications systems, to state-of-the-art microprocessor design, to space-borne computers, to industrial controls. Mr. McCabe has been responsible for the creation of a VHDL-based design methodology at a number of companies. On various projects, Mr. McCabe has held positions of lead hardware engineer, lead verification engineer and lead systems engineer. Mr. McCabe has also taught internal classes at various companies on VHDL-based design techniques.

Mr. McCabe has presented papers on bus functional model design and system simulation at the VHDL International User's Forum (VIUF), and has also been a session chair for that conference.

Mr. McCabe holds both Bachelor of Science and Master of Science degrees in Computer Engineering. He holds a U.S. patent for the design of a frame relay ASIC, and is also a member of the IEEE.

Mike Kowalski, Consultant

Mr. Kowalski specializes in HDL based top-down design methodology, synthesis, and ASIC verification. Mr. Kowalski has held responsibilities for many system, architecture, and block-level ASIC designs, as well as leading verification efforts and designing verification methodologies and strategies for several ASIC developments. In execution of these duties, Mr. Kowalski has gained extensive experience in simulators, synthesis tools, coverage tools, model development, emulators, and chip testers.

Michael Kowalski has 25 years of development experience, with 20 years in ASIC and FPGA design for companies such as Honeywell, AT&T, Paradyne, Cirrus Logic, and Intel.

Mr. Kowalski has experience with a variety of fabrication vendors, including GE, AMI, VLSI Tech, IBM, Samsung, Texas Instruments, and AT&T (Lucent), providing a broad view of the industry. Mr. Kowalski has experience in device complexity ranging from simplistic functions to very large and complex system on a chip designs with multiple embedded cores.

Mr. Kowalski has a BSEE from MSOE, is a member of the IEEE, and holds a patent for a DSL processor design.