

## **Verilog Course Developers and Instructors**

TM Associates (TMA) believes that the best training is developed and delivered by people who are not only language experts but also have years of design experience. And instead of relying on one person and a single point of view TMA uses the team approach to develop training.

TMA has assembled a group of Verilog experts with over 45 years of Verilog experience. The following people developed our Verilog training.

### **Mike Ciletti Ph.D., Professor of Electrical and Computer Engineering, University of Colorado**

Dr. Ciletti is a professor of electrical and computer engineering at the University of Colorado at Colorado Springs. He has developed and presented several short courses to engineers in the United States, Asia and Europe treating the design and synthesis of application specific integrated circuits (ASICs) using Verilog, and is active as a consultant for Verilog-based modeling and synthesis. He also developed and presented several short-courses at the annual meetings of Open Verilog International (now Accellera) and was a balloting member for IEEE Std. 1364-1995.

Dr. Ciletti is the author of the following well-respected verilog textbooks:

- *Modeling, Synthesis, and Rapid Prototyping with the Verilog HDL*
- *Advanced Digital Design with the Verilog HDL*
- *Starter's Guide to Verilog 2001*

### **Steven E. Start , Independent Consultant**

Mr. Start has over 15 years of engineering experience in electrical engineering and software development. He possesses a broad range of practical engineering experience including real-time embedded systems development, EDA Tool technical support, EDA library development, front and back-end digital ASIC design methodology development, and industrial instrumentation and control. His career includes working for Argonne National Laboratory and AMI Semiconductor, and work as a consultant. While at AMI Semiconductor, he prepared and taught several classes on EDA point-tools and design flow. Mr. Start has authored and co-authored several original technical papers, two of which received Synopsys User's Group 1st place best paper awards (Boston 2000, 2001). Mr. Start was a balloting member of the IEEE Design Automation Standard Committee and participated in the IEEE 1364 Verilog Hardware Description Language standard revision

(2001). He served as a technical committee member for the International Symposium on Quality Electronic Design (ISQED) including serving as chairman and co-chairman for the EDA Tools/Design Methodology Subcommittee in 2000 and 2001. He holds a Bachelor of Science in Electrical Engineering and a Master of Science degree in Computer Engineering. Steve currently contracts engineering design work related semiconductor work as an independent contractor.

#### **Charles Dancak, Independent Consultant**

Mr. Dancak is an independent consultant and course developer specializing in HDL-based ASIC/FPGA synthesis and DFT. Mr. Dancak spent ten years at Synopsys, where he developed several of that company's most highly-rated and successful customer-training workshops. Prior to joining Synopsys, he was employed at Cadence, Teradyne, Silicon Compilers, and Intel. He has traveled across North America, Europe, and Asia, presenting EDA workshops and seminars to hundreds of design engineers interested in getting the most out of the languages and their tools.

Mr. Dancak has worked with Verilog and VHDL since 1992, is fluent in both, and currently teaches basic and advanced extension classes in HDL-based design and verification at the University of California, Santa Cruz. He has an MSEE from the University of Wisconsin, and an MS in Solid-State Physics from the Polytechnic University of New York.

#### **Chuck Mangan, Independent Consultant**

Mr. Mangan is an electrical engineer with 20 years experience in design, manufacturing, test, and project management. He is considered an authority in IC Verification using Verilog, Specman, and Vera and in IC Design using Verilog. Mr. Mangan has worked on and managed IC and FPGA design and verification projects from 10,000 to 20M gates. He has presented at conferences and is the author of the well known "e Language Field Guide".

Mr. Mangan has also used his expertise to instruct many engineers in the art and methodology of verification and reuse via beginning and expert classes in designing with Verilog and in verification using Verilog, Specman, and Vera. He continues to work as a consultant now through his own company, and teaches classes in design and verification for TM Associates.