

High Speed Interconnect Design

2 Days

50% Lecture, 50% Labs

Intermediate Level

Overview

As design speeds continue to increase Signal Integrity become more and more of an issue. High Speed Interconnect Design covers basic and advanced Signal Integrity (SI) concepts which determine when SI must be considered and addressed as part of the design equation. Termination techniques, PCB stackup and bus topology impacts are discussed. Further, an overview of available models is presented. The critical factors in GBit design are introduced including a discussion on S-Parameters. Students interactively use the Hyperlynx SI CAD tool as the lab basis to learn high speed SI principles.

Benefits

Upon completing this targeted training, students will have the necessary skills to understand:

- How SI effects arise and when they are critical
- The basics of IBIS and HSPICE simulations
- Effective transmission line termination and topology techniques
- How parasitics effect signal characteristics
- The impact of PCB structures such as the stackup, vias and loss
- The critical concepts in GBit designs
- Additionally, student SI problems are entertained as time permits.

Intended audience

Any designer using modern technology parts is a candidate for SI scrutiny. Those individuals working on digital designs who must have the knowledge to implement them correctly. This includes digital designers, board layout designers as well as any entrepreneurial individual who needs to understand what is involved and how to implement high speed interfaces.

Prerequisites

No previous knowledge is assumed. Basic mathematics are utilized in conjunction with CAD tool analysis.

Course Outline

Day 1

- What is a transmission line?
- The nature of inductance
- The nature of capacitance
- Interactive use of Hyperlynx to explore a TLine
- An exploration of IBIS and SPICE models
- Interactive use of Hyperlynx to design clock topologies
- Differential signaling basics

Day 2

- Parasitics, where do they come from

- Interactive lab on parasitic reactions
- The PCB stackup and its ramifications
- Crosstalk
- Interactive lab on PCB structures and XTLK
- Bus structures
- Parameters for an overall design
- Interactive lab to discuss bus structures and SI design of SDRAM interface
- Critical issues for successful GBit links
- Introducing S-parameters

Developer and Instructor: Nick Krull

Nick Krull has an MSEE from the University of North Carolina and has been engaged in design engineering for IBM, StorageTek, Xilinx and BOC Medical for the past 25 years.

Mr. Krull's design background includes involvement in the design of such products as printers, high performance fibre channel storage controllers and medical instrumentation. Mr. Krull has led teams of engineers through product development cycles, giving him a unique understanding and perspective on product development

Since 1999 Mr. Krull has provided SI consulting services through his company Electronic Expertise, helping companies implement high speed parallel and multi gigabit serial links, high speed processor implementations DDR and RLDRAM designs as well as serial multi-gigabit links.

Mr. Krull's clients have included McData, Xilinx, StorageTek, Cisco, Intel, IBM, AMD and Kodak.

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